

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. TI-33423A		SERIAL NO. TBD 10/762,163	
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>								
					APPLICANT: Yunus et al.			
					FILING DATE Herewith		GROUP 2824 TBD	
U.S. PATENT DOCUMENTS								
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)	
Beo		US 6,213,347 B1	04/10/01	Thomas	222	52	04/30/1999	
		US 6,228,680 B1	05/08/01	Thomas	438	108	05/01/1999	
		US 6,245,583 B1	06/12/01	Amador et al.	438	14	04/30/1999	
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FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SU B CL AS S	TRANSLATION	
							YES	NO
OTHER NON-PATENT DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>								
Beo		"A Silicon and Aluminum Dynamic Memory Technology" Larsen, IBM J. Res. Develop. Vol 24. No. 3, May 1980, pp. 258-282						
		"Calculated Thermally Induced Stresses In Adhesively Bonded and Soldered Assemblies" Suhir, AT&T Bell Laboratories, Murray Hill, New Jersey 07974, pp. 383-392						
		"Clasp Ceramic Column Grid Array Technology for Flip Chip Carriers", Ray et al., Advanced Packaging Technologies Tutorial, SEMICON West 99, pp. A-1 - A-7						
		"Controlled Collapse Reflow Chip Joining", Miller, IBM Components Division, May 1969, pp. 239-250						
		"Die Attachment Design and Its Influence on Thermal Stresses, Suhir, AT&T Bell Laboratories, Murray Hill, New Jersey 07974, pp. 508-517						
		"Geometric Optimization of Controlled Collapse Interconnections", Goldmann, IBM Components Division, Fishkill, New York, May, 1969, pp. 251-265						
		"Reliability of Controlled Collapse Interconnections", Norris et al., IBM Components Division, May, 1969, pp. 266-271						
		"SLT Device Metallurgy and Its Monolithic Extension", Totta et al., IBM J. Res. Develop. May 1969, pp. 226-238.						
		"Studies of the SLT Chip Terminal Metallurgy", Berry et al., IBM J. Res. Develop., May 1969, pp. 286-296						
		"The Quality of Die-Attachment and Its Relationship to Stresses and Vertical Die-Cracking", van Kessel, et al., 1983 IEEE, pp. 237-244						
Beo		"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Oktay, IBM Components Division, May 1969, pp. 272-285						
EXAMINER Brian E. Owens					DATE CONSIDERED 8.22.04			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								